In the Claims:

Claim 1 (currently amended): A method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size, the method comprising:

measuring a first time period related to erasing the first sector;

establishing a first test limit based on the first time period;

measuring a second time period related to erasing the second sector;

establishing a second test limit based on the second time period; and

determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test.

Claim 2 (currently amended): The method of Claim 1, wherein the semiconductor device comprises a plurality of first sectors and a plurality of second sectors, and the first test limit is based on an average of first time periods associated with the first time period for each of the first sectors and the second test limit is based on an average of second time periods associated with the second time period for each of the second sectors.

Claim 3 (currently amended): The method of Claim 1 further comprising:

measuring a third time period related to erasing the first sector; and

measuring a fourth time period related to erasing the second sector, the first and second time periods being erase time periods[,]; and the third and fourth time periods being auto program disturb erase~~APDE~~ time periods, the first test limit being based on at least one of[:] the first and third time periods[,]; the second test limit being based on at least one of[:] the second and fourth time periods.

Claim 4 (previously presented): The method of Claim 3, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 5 (currently amended): The method of Claim 2 further comprising:

measuring a third time periods related to erasing each of the plurality of first sectors; and

measuring a fourth time periods related to erasing each of the plurality of second sectors, the first and second time periods being erase time periods; and the third and fourth time periods being ~~APDE~~auto program distrub erase time periods, the first test limit being based on at least one of[:] the first and third time periods[,]; the second test limit being based on at least one of[:] the second and fourth time periods.

Claim 6 (previously presented): The method of Claim 5, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 7 (previously presented): The method of Claim 1, wherein the act of determining includes determining whether a time period associated with erasing the first sector exceeds the first test limit and whether a time period associated with erasing the second sector exceeds the second test limit.

Claim 8 (currently amended): The method of Claim 1, further comprising executing at least one parameter test on the device, wherein said at least one parameter test is selected from the group consisting of a test for open circuits, a test for short circuits, a test for electrical leakage, and a device signature test.

Claim 9 (original): The method of Claim 1, wherein the second sector is a boot sector.

Claim 10 (currently amended): A system for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size, the system comprising:

a measuring element configured to measure a first time period related to erasing the first sector, the measuring element further configured to measure a second time period related to erasing the second sector;

an establishing element configured to establish a first test limit based on the first time period, the establishing element further configured to establish a second test limit based on the second time period; and

a determining element configured to determine whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test.

Claim 11 (previously presented): The system of Claim 10, wherein the device comprises a plurality of first sectors and a plurality of second sectors, and the first test limit is based on an average of first time periods associated with the first time period for each of the first sectors and the second test limit is based on an average of second time periods associated with the second time period for each of the second sectors.

Claim 12 (currently amended): The system of Claim 10, wherein the measuring element is further configured to measure a third time period related to erasing the first sector and a fourth time period related to erasing the second sector, and wherein the first and second time periods being erase time periods and the third and fourth time periods being ~~APDE~~auto program disturb erase time periods[,]; the first test limit being based on

at least one of[:] the first and third time periods[,]; the second test limit being based on at least one of[:] the second and fourth time periods.

Claim 13 (previously presented): The system of Claim 12, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 14 (currently amended): The system of Claim 11, wherein the measuring element is further configured to measure a third time period related to erasing each of the plurality of first sectors and a fourth time period related to erasing each of the plurality of second sectors, the first and second time periods being erase time periods and the third and fourth time periods being ~~APDE~~auto program disturb erase time periods[,]; the first test limit being based on at least one of[:] the first and third time periods[,]; the second test limit being based on at least one of[:] the second and fourth time periods.

Claim 15 (previously presented): The system of Claim 14, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 16 (previously presented): The system of Claim 10, wherein the determining element determines whether a time period associated with erasing the first

sector exceeds the first test limit and whether a time period associated with erasing the second sector exceeds the second test limit.

Claim 17 (currently amended): The system of Claim 10, wherein the system executes at least one parameter test on the device, wherein said at least one parameter test is selected from the group consisting of a test for open circuits, a test for short circuits, a test for electrical leakage, and a device signature test.

Claim 18 (previously presented): The system of Claim 10, wherein the second sector is a boot sector.